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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

SHARAD KAPUR, et al.

Serial No.:

09/427,238

Filed:

October 26, 1999

For:

A SOFTWARE ANALYSIS TOOL FOR LARGE SCALE CAPACITANCE

CALCULATIONS FOR INTEGRATED CIRCUITS

Group No.:

2858

Examiner:

N/A

Commissioner of Patents and Trademarks Washington, D. C. 20231

Sir:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 3/24/00 (Date)

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Signature of the person signing the certificate)

3/24/00 (Date of Signature)

INFORMATION DISCLOSURE STATEMENT

Pursuant to the duty of disclosure under 37 C.F.R. § 1.56, Applicant submits this statement. This submittal is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure. The patents, publications and other information herein are listed below and on the attached Form PTO-1449. Copies of the listed references are submitted herewith.

References:

"GMRES: A GENERALIZED MINIMAL RESIDUAL ALGORITHM FOR SOLVING NONSYMMETRIC LINEAR SYSTEMS," by Y. Saad and M. H. Shultz, SIAM Journal on Scientific and Statistical Computing, 7(3):856-69, 1986

"INTRODUCTION TO NUMERICAL ANALYSIS," by J. Soer and R. Bulirsh, Springer-Verlag 1979 and in" PRECONDITIONED, ADAPTIVE, MULTIPOLE-ACCELERATED ITERATIVE METHODS FOR THREE-DIMENSIONAL FIRST-KIND INTEGRAL EQUATIONS OF POTENTIAL THEORY," by K. Nabors, et al., SIAM Journal on Scientific and Statistical Computing, 15(3):713-735, May 1994

Applicant hereby expressly reserves the right to swear behind the effective dates of any of the above Patents and to question the relevance and materiality of the Patents and Publications listed herein, in whole, in part, or in combination, subsequent to filing this Information Disclosure Statement.

Respectfully submitted,

HITT CHWANG & GAINES, P.C.

David H. Hith

Registration No. 33,182

Date: MARCH 24, 2000

P.O. Box 832570 Richardson, Texas 75083 (972) 480-8800